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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/340,580	06/28/1999	CHUNG-WAH NORRIS IP	21891.01700	4118

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EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/340,580	Applicant(s) Chung-Wah Norris Ip
	Examiner Thai Phan	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 28, 1999* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-36* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office action is response to patent application S/N: 09/340,580. Claims 1-36 are pending in this official action.

Drawings

1. This application has been filed with drawings which are acceptable for examination (see enclosed form PTO 948).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maston, US patent no. 5,323,401.

As per claim 1, Maston discloses method and system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 5), recording simulation data to produce corrective action and valid stimulus test vector (col. 3, line 18 to col. 4, line 47) from the first

analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed in col. 3.

As per claim 2, Maston discloses deriving a new set of stimulus data from previously recorded simulation data or simulation history.

As per claim 3, Maston discloses sequence of stimulus vector or portion of test sequence would be used to apply to region verification efficiency (col. 3, lines 1-17, col. 5, for example).

As per claim 4, Maston discloses method and system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test method includes steps of dividing all or each possible design states for the design into a plurality of interest validation regions (col. 5), recording simulation data to produce corrective action and valid stimulus test vector (col. 3, line 18 to col. 4, line 47) for each of the validation regions from the first analysis step, and generating or transforming a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed in col. 3.

As per claim 5, Maston discloses simulation efficiency and state coverage during simulation (cols. 3-4).

As per claim 6, Maston discloses generating new stimuli, test vectors, data transformation for use in valid test (col. 3).

As per claim 7, Maston discloses occurrence of the taken stimulus in the current validation (col. 4), using the current stimulus for subsequent steps if needed to valid a test (col. 3, lines 18-30), and timing restriction rules such as occurrence rules, check states, etc. for stimulus data applied for test validation (col. 5).

As per claim 8, Maston discloses stimulus specification, and state legal for valid test (cols. 3-5).

As per claim 9, Maston discloses current update for simulation test data.

As per claim 10, due to the similarity of claim 10 to claim 1, claim 10 is therefore rejected under the same rationales as set forth in claim 1.

As per claims 11 and 12, Maston discloses occurrence of the taken stimulus in the current validation (col. 4), using the current stimulus for subsequent steps if needed to valid a test (col. 3,

lines 18-30), and timing restriction rules such as occurrence rules, check states, etc. for stimulus data applied for test validation (col. 5).

As per claim 13, Maston discloses method and system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test method includes steps of dividing or partitioning all possible design states for the design into a plurality of interest validation regions (col. 5), recording simulation data to produce corrective action and valid stimulus test vector (col. 3, line 18 to col. 4, line 47) from the first analysis step, and means for generating or transforming a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed in col. 3.

As per claims 14-18, due to the similarities of claims 14-18 to claims 1, 3 and 7 above, claims 14-18 are also rejected under the same rationales as set forth.

As per claim 19, Maston discloses method and system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test system includes means for performing steps of dividing all or each

possible design states for the design into a plurality of interest validation regions (col. 5), recording simulation data to produce corrective action and valid stimulus test vector (col. 3, line 18 to col. 4, line 47) from the first analysis step, and generating or transforming a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed (see col. 3).

As per claim 20, Maston discloses means for deriving a new set of stimulus data from previously recorded simulation data or simulation history

As per claim 21, Maston discloses means for changing the order in the existing stimuli based the previously recorded simulation data or simulation history as claimed (col. 3, and col. 5),

As per claim 22, Maston discloses system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test system includes means for performing steps of dividing all or each possible design states for the design into a plurality of interest validation regions (col. 5), means for recording simulation data to produce corrective action and valid stimulus test vector (col. 3,

line 18 to col. 4, line 47) from the first analysis step for each of the validation regions, and generating or transforming a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed in col. 3.

As per claims 23-27, claims 23-27 are directed to system for performing steps and system for performing method claims 5-9, claims 23-27 are thus rejected under the same rationales as set forth.

As per claim 28, Maston discloses system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test system includes means for performing steps of dividing all or each possible design states for the design into a plurality of interest validation regions (col. 5), recording simulation data to produce corrective action and valid stimulus test vector (col. 3, line 18 to col. 4, line 47) from the first analysis step, and generating or transforming a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed in cols. 3-5..

Similarly, claims 29-30 are directed to system for performing steps of method claims 2-3 and 7 above, claims 29-30 are thus rejected in like manner.

As per claims 31-36, claims 31-36 are directed to system for performing steps of claims 13-16 above. And Maston discloses method and system for testing and verifying circuit design with feature limitations very similar to the claimed invention (Summary of the Invention). According to Maston, the test system includes means for performing steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 5), recording simulation data to produce corrective action and valid stimulus test vector (col. 3, line 18 to col. 4, line 47) from the first analysis step for each divided regions, and means for generating or transforming a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 3-5). Maston does not expressly disclose simulation history data as claimed.

Practitioner in the art at the time of the invention would have found recorded data from the first simulation analysis to derive stimuli obviously implies claimed simulation history because data previously recorded in the first analysis was historic data and such previously

recorded simulation data or historic simulation data was used to derive for new set of stimuli for corrective action and valid test in the second analysis as disclosed in col. 3 and col. 5.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Patent no. 4,745,355, issued to Eichelberger et al., on May 1988
2. Patent no. 4,817,093, issued to Jacobs et al., on Mar. 1989
3. Patent no. 5,638,383, issued to Wotzak et al., on June 1997
4. Patent no. 5,825,785, issued to Barry et al., Oct. 1998
5. Patent no. 5,867,399, issued to Rostoker et al., Feb. 1999
6. Patent no. 5,966,306, issued to Nodine et al., Oct. 1999
7. Patent no. 5,920,830, issued to Hatfield et al., July 1999

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

September 29, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER